Superbend Controls Design Requirements 8/2/99

Background

The ALS control system consists of a collection of commercial and custom micro based computers.

consoles	PC and Sun
servers	PC and Sun
realtime i/o	custom "ILC" Intelligent Local Controller (450 each)
	VME (srioc, beamlines)
	Compact PCI (third harmonic cavity)
legacy core	Multibus I "CMM" Collector Multi Micro
	Multibus II "DMM" Display Micro Module

Upgrade in Progress

We are currently in the process of engineering an upgrade to an expanded, more maintainable and capable system. This with near-zero downtime, maintenance of all features, and a very long set of nontrivial requirements. The requirements are to do this smoothly and within available resources.

The plans for ALS controls expansion and upgrade is only partly based on performance requirements. The actual performance required at the ALS is in most cases so low that is not the primary criterion. The design is driven by other requirements, such as the project requirement of having I/O on the rear of the chassis which moved us in the direction of Compact PCI rather than the VME that had been the evolutionary choice. In the processor arena most any cpu that has support from the realtime OS VxWorks, another existing standard.

Since the ALS is a very longterm project we must select commercial equipment that can be supported and upgraded over a long period of time with minimum life cycle cost.

We selected a Motorola PowerPC based processor that has good cost/performance, has the realtime support we require, and does not have a heat problem in a confined chassis. Motorola has a very good reputation for stability and long life cycle on their board products. This is a case where the final selection of the process was not as expected, but fits the requirements better than the predicted outcome. This indicates to me that the system requirements and design process is working, and not merely rubber-stamping the initial expectations of the team.

This processor has far greater capability than we require in anything on the machine (so far), but there is really no way to save a few dollars here by lowering the performance. The cost of these in the plan is insignificant anyway, even if we found a cheaper cpu. The support cost and additional software licenses, and the inventory and maintenance sparing would not be worthwhile. And the additional performance is usually found to be useful or necessary for an improvement later on.

The I/O card we are using is one built under our direction. Initially we expected to use commercial boards, and in many cases we do, but for the upgrade of the machine we must pattern our I/O after the existing 450 homebuilt Intelligent Local Controllers (ILC). They have a mix of I/O and are deployed in variable numbers at each chassis, so we need a mix of I/O that is equal or greater, else the cable wiring becomes expensive, complex, and incompatible. No existing commercial boards we found met these requirements. We built the minimum hardware - an IP based card that uses a commercial IP carrier to interface with the cPCI bus. We have the boards fabricated and assembled commercially and we do the parts procurement and testing. We are discussing having

them completely built and cataloged by a vendor, but the batch we built (for Harmonic Cavity) and the new one for Superbend we will coordinate the manufacturing due to schedule control. The coordinator and engineer working on this also did the original ILCs, so they have intimate experience with ALS requirements and systems, as well as the design and manufacture of them.

The controls expansion approach was first tested on the Harmonic Cavity system. Two Compact PCI chassis were installed and are controlling this system in production.

New Requirements of the Superbends

The superbends present several new requirements to the control system. The most significant is the need for full 16 bit accuracy and stability, this gives no margin for the hardware standardized there. For this reason it was chosen to use more than 16 bit accuracy (18) and communicate with the power supply via a digital means so to avoid the analog cabling and inherent problems at this level.

Additionally the Quadrupole magnet controls are standard, but we do not have the Legacy control hardware to use on them, so we will control them with the new hardware. This represents a change but one that was expected in the flow of things and should present no significant challenge. Some code will be ported from the ILC system to the cPCI to make the behavior of the controls as similar as possible to the rest of the magnets.

Aside from the usual additional channels there is only the GPIB interfacing to the Teslameters, and a new control room application customized to the needs of the superconducting magnets.